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2 40-mm² 3-V-only 50-MHz 64-Mb 2-b/cell CHE NOR flash memory
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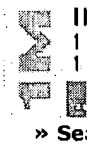
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Kirihata, T.; Gall, M.; Hosokawa, K.; Dortu, J.-M.; Hing Wong; Pfefferer, P.; Ji, Weinfurter, O.; DeBrosse, J.K.; Terletzki, H.; Selz, M.; Ellis, W.; Wordeman, Kiehl, O.;

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Pages:1711 - 1719

[\[Abstract\]](#) [\[PDF Full-Text \(192 KB\)\]](#) IEEE JNL

25 Linear search algorithm for repair analysis with 4 spare row/4 spare column

Hyeokman Kwon; Joohyeong Moon; Jinsoo Byun; Sangwook Park; Jinyong Ch ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on , 28-30 Aug. 2000

Pages:269 - 272

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) IEEE CNF

26 Analysis of a hybrid defect-tolerance scheme for high-density mem

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31 An approach for online repair and yield enhancement of VLSI/WSI redundant memories
Shen, Y.-N.; Lombardi, F.;

CompEuro '91. 'Advanced Computer Technology, Reliable Systems and Applications'. 5th Annual European Computer Conference. Proceedings. , 13-1 May 1991

Pages:685 - 689

[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) **IEEE CNF**
32 Wafer scale integration (WSI) of programmable gate arrays (PGA's
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Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 23-25 Jan. 1990

Pages:329 - 338

[\[Abstract\]](#) [\[PDF Full-Text \(588 KB\)\]](#) **IEEE CNF**
33 A 50 ns 16 Mb DRAM with a 10 ns data rate
Kalter, H.; Barth, J.; D Lorenzo, J.; Drake, C.; Fifield, J.; Hovis, W.; Kelley, G., Lewis, S.; Nickel, J.; Stapper, C.; Yankosky, J.;

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[\[Abstract\]](#) [\[PDF Full-Text \(720 KB\)\]](#) **IEEE CNF**
34 Approaches for the repair of VLSI/WSI RRAMs by row/column dele
Lombardi, F.; Huang, W.K.;

Fault-Tolerant Computing, 1988. FTCS-18, Digest of Papers., Eighteenth

International Symposium on , 27-30 June 1988
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[\[Abstract\]](#) [\[PDF Full-Text \(444 KB\)\]](#) **IEEE CNF**

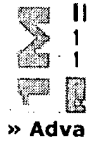
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<sentence> column) <and>
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<sentence> row)
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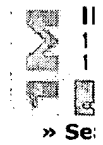
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<phrase> (method <or> process
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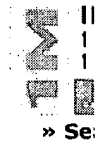
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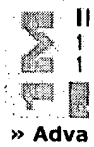
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1 A 3.3-V 12 ns 16 Mb CMOS SRAM

Goto, H.; Ohkubo, H.; Kondou, K.; Ohkawa, M.; Mitani, H.; Horiba, S.-I.; Soe M.; Hayashi, F.; Hachiya, Y.; Shimizu, T.; Ando, M.; Matsuda, Z.;
 Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC 1992 IEEE International , 19-21 Feb. 1992
 Pages:216 - 217, 288

[\[Abstract\]](#) [\[PDF Full-Text \(204 KB\)\]](#) **IEEE CNF**
2 Built in self repair for embedded high density SRAM

Ilyoung Kim; Zorian, Y.; Komoriya, G.; Pham, H.; Higgins, F.P.; Lewandowski,
 Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
 Pages:1112 - 1119

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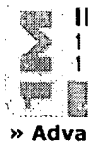
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(sram <or> ram <or> dram <or>
memory) <and> ((bist <or>
self-test <or> (self <phrase>
test)) <phrase> (method <or>
```


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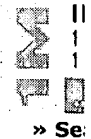
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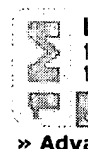
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- 3) Limit the results by selecting Search Options.
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```
((bist <or> self-test <or>
(self <phrase> test))
<phrase> (method <or> process
<or> procedure)) <and>
```

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```
(sram <or> ram <or> dram <or>
memory) <and> (bist <or> self-
test <or> (self <phrase>
test)) <and> ((redundant <or>
```


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1 SRAM embedded memory with low cost, flash EEPROM-switch-contr redundancy

McPartland, R.J.; Loeper, D.J.; Higgins, F.P.; Singh, R.; MacDonald, G.; Komo G.; Aymeloglu, S.; DePaolis, M.V.; Leung, C.W.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE
2000 , 21-24 May 2000
Pages:287 - 289

[\[Abstract\]](#) [\[PDF Full-Text \(240 KB\)\]](#) **IEEE CNF**

2 A 3.3-V 12 ns 16 Mb CMOS SRAM

Goto, H.; Ohkubo, H.; Kondou, K.; Ohkawa, M.; Mitani, H.; Horiba, S.-I.; Soe M.; Hayashi, F.; Hachiya, Y.; Shimizu, T.; Ando, M.; Matsuda, Z.; Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC 1992 IEEE International , 19-21 Feb. 1992
Pages:216 - 217, 288

[\[Abstract\]](#) [\[PDF Full-Text \(204 KB\)\]](#) **IEEE CNF**

3 Built in self repair for embedded high density SRAM

Ilyoung Kim; Zorian, Y.; Komoriya, G.; Pham, H.; Higgins, F.P.; Lewandowski,
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:1112 - 1119

[\[Abstract\]](#) [\[PDF Full-Text \(540 KB\)\]](#) **IEEE CNF**



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- 1 A new column redundancy scheme for fast access time of 64-Mb DR.**
Jun, Y.-H.; Jeong, W.-H.; Park, J.-H.; Kim, T.-H.; Kim, S.-W.; Lee, J.-S.; Jang J.; Khang, C.-M.; Lee, H.-G.;
 Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium
 on , 3-6 May 1993
 Pages:1937 - 1940 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(264 KB\)\]](#) **IEEE CNF**

- 2 A 1.6-GByte/s DRAM with flexible mapping redundancy technique and an additional refresh scheme**
Takase, S.; Kushiyama, N.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 11 , Nov. 1999
Pages:1600 - 1606

[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) **IEEE JNL**

- 3 A flexible redundancy technique for high-density DRAMs**
Horiguchi, M.; Etoh, J.; Aoki, M.; Itoh, K.; Matsumoto, T.;
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 1 , Jan. 1991
Pages:12 - 17

[\[Abstract\]](#) [\[PDF Full-Text \(508 KB\)\]](#) **IEEE JNL**

- 4 Column redundancy scheme for multiple I/O DRAM using mapping t**
Yong-Weon Jeon; Young-Hyun Jun; Suki Kim;
 Electronics Letters , Volume: 36 , Issue: 11 , 25 May 2000
 Pages:940 - 942

[\[Abstract\]](#) [\[PDF Full-Text \(481 KB\)\]](#) **IEE JNL**

5 0.13- μ m 32-Mb/64-Mb embedded DRAM core with high efficient redundancy and enhanced testability

Kikukawa, H.; Tomishima, S.; Tsuji, T.; Kawasaki, T.; Sakamoto, S.; Ishikawa, Abe, W.; Tanizaki, H.; Kato, H.; Uchikoba, T.; Inokuchi, T.; Senoh, M.; Fukus, Y.; Nirro, M.; Maruta, M.; Shibayama, A.; Ooishi, T.; Takahashi, K.; Hidaka, H.
Solid-State Circuits, IEEE Journal of , Volume: 37 , Issue: 7 , July 2002
Pages:932 - 940

[[Abstract](#)] [[PDF Full-Text \(389 KB\)](#)] IEEE JNL

6 Dynamically shift-switched dataline redundancy suitable for DRAM macro with wide data bus

Namekawa, T.; Miyano, S.; Fukuda, R.; Haga, R.; Wada, O.; Banba, H.; Take, S.; Suda, K.; Mimoto, K.; Yamaguchi, S.; Ohkubo, T.; Takato, H.; Numata, K.
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 5 , May 2000
Pages:705 - 712

[[Abstract](#)] [[PDF Full-Text \(440 KB\)](#)] IEEE JNL

7 SEU-hardened silicon bipolar and GaAs MESFET SRAM cells using loc redundancy techniques

Hauser, J.R.;
Nuclear Science, IEEE Transactions on , Volume: 39 , Issue: 1 , Feb. 1992
Pages:2 - 6

[[Abstract](#)] [[PDF Full-Text \(396 KB\)](#)] IEEE JNL

8 Optimized redundancy selection based on failure-related yield mode 64-Mb DRAM and beyond

Kikuda, S.; Miyamoto, H.; Mori, S.; Niir, M.; Yamada, M.;
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 11 , Nov. 1991
Pages:1550 - 1555

[[Abstract](#)] [[PDF Full-Text \(576 KB\)](#)] IEEE JNL

9 SRAM embedded memory with low cost, flash EEPROM-switch-contr redundancy

McPartland, R.J.; Loeper, D.J.; Higgins, F.P.; Singh, R.; MacDonald, G.; Komo, G.; Aymeloglu, S.; DePaolis, M.V.; Leung, C.W.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
Pages:287 - 289

[[Abstract](#)] [[PDF Full-Text \(240 KB\)](#)] IEEE CNF

10 Integration of SRAM redundancy into production test

Jayabalan, J.; Povazanec, J.;
Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002
Pages:187 - 193

[[Abstract](#)] [[PDF Full-Text \(426 KB\)](#)] IEEE CNF

11 Dynamically shift-switched dataline redundancy suitable for DRAM macro with wide data bus

Namekawa, T.; Miyano, S.; Fukuda, R.; Haga, R.; Wada, O.; Banba, H.; Take, S.; Suda, K.; Mimoto, K.; Yamaguchi, S.; Ohkubo, T.; Takato, H.; Numata, K.
VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on , 17-19 : 1999

Pages:149 - 152

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) [IEEE CNF](#)

12 A 1.6 GB/s DRAM with flexible mapping redundancy technique and additional refresh scheme

Takase, S.; Kushiya, N.;
Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International , 15-17 Feb. 1999

Pages:410 - 411

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) [IEEE CNF](#)

13 A defect and fault tolerant design of WSI static RAM modules

Tsuda, N.;
Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 23-25 Jan. 1990

Pages:213 - 219

[\[Abstract\]](#) [\[PDF Full-Text \(288 KB\)\]](#) [IEEE CNF](#)

14 I/O divided column redundancy scheme for high-speed DRAM with multiple I/Os

Jae-Goo Lee; Young-Hyun Jun; Chilgee Lee; Bai-Sun Kong;
Electronics Letters , Volume: 36 , Issue: 24 , 23 Nov 2000

Pages:1996 - 1997

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) [IEEE JNL](#)

15 Redundancy techniques for high-density DRAMs

Horiguchi, M.;
Innovative Systems in Silicon, 1997. Proceedings., Second Annual IEEE International Conference on , 8-10 Oct. 1997

Pages:22 - 29

[\[Abstract\]](#) [\[PDF Full-Text \(500 KB\)\]](#) [IEEE CNF](#)

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And 

(second <phrase> pas In: All Fields

And

(row <phrase> failure) In: All Fields

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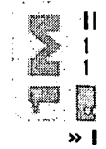


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(first <phrase> pass)	In: All Fields
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And 

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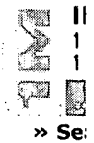
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